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PULSE AMPLITUDE ANALYZER

by

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An amplitude analyzer with a system of storage on magnetic cores is described, certain methods of construction of the ferrite memory section are covered. A block diagram of a translator of input signals is given, which more fully answers the requirements of a modern pulse analyzer. The overall characteristics of an apparatus constructed in 1955 on the basis of the principles under consideration, are given.

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BLOCK DIAGRAM OF THE AMPLITUDE ANALYZER

A block diagram of the analyzer is shown in Fig. 1 and a general view in Fig. 2.

An amplified signal from the particle counter is fed into the input of the analyzer. The pulse under investigation is transformed in the translator section, into a train of standardized pulses, whose number (from 1 to 100) is proportional to the amplitude of the input signal and is equal to the number of the channel in which the signal arriving at the input must be registered [1].

The train of standardized pulses is fed to channel selector circuit which consists of two ring systems, each of which is a decade counter. The "memory" of the analyzer, operating with ferrite cores, serves to store the number of pulses entering each channel.

The data storage process consists of the following. After channel selection, the number previously stored in it, is removed from the memory and is fed into the adder section. The adder adds one to the entered number, and the newly obtained number is introduced back into the "memory." Upon completion of the measurement process, the received data can be displayed, on a linear scale, on the screen of a cathode ray tube [2].

The numerical values of the spectrum under investigation are picked off the adder indicators, the sequence of all operations is determined by the programming section.

THE MEMORY SECTION

In the development of the memory section, three systems of ferrite hook-ups were investigated: the system of coincidence of two currents, the system of total current, and the system of coincidence of three currents.

System of Coincidence of Two Currents. If the shape of the hysteresis curve of the magnetic core is such that a current pulse of an amplitude equal to 1/2 I of either polarity does not produce magnetic reversal of the core, then such ferrite can operate on the system of the coincidence of two currents [2,3]. The core must in this case have two windings through which will pass the half-current pulses, in which event reversal is possible upon coincidence of two currents (Fig. 3, A).

In the memory section under consideration a matrix having 10 rows and 10 columns is used. The numbers of these rows and columns constitute the XY coordinates of the corresponding channel of the matrix (Fig. 3, B).

Besides the two groups of windings XY, as indicated, there are two more common windings in the matrix. One of these, the output winding, passes through all the diagonals in series with all the ferrites. By means of the amplitude of the pulse induced in this winding by a saturated core, it is possible to determine which numbers are remembered by this or that ferrite (Fig. 3, E). For the purpose of increasing the ratio of the pulse amplitudes corresponding to states 1 and 0, the output pulses are fed into coincidence circuits with a strobe pulse (Fig. 3, E).

In a 10 × 10 matrix it is possible to record and count one hundred different binary numbers, i.e., zeroes and ones. In order to store the same quantity of numbers with values up to 2^N, N such matrices are required. From these a pile is assembled in such a manner that all the rows and columns with the same numbers are connected in series (Fig. 3, C).

From each matrix, the pulses induced in the output windings are amplified, strobed and fed to the anodes of the adder triggers. Prior to the moment of read-out the adder is reset to 0. On read-out the drivers of those coordinates on which I's were written are turned over by pulses arriving from the coincidence circuits. In this manner, the number, which was registered in the memory, is collected in the adder.

After read-out a single pulse is fed into the input of the adder, that is one is added to the number. Following this, the newly obtained number must be written into the same channel, for which purpose, pulses corresponding to read-in of one are applied to the X and Y windings of the channel selected. However, on some of the units zeroes must be written in. For this reason, each matrix has a so-called Z-winding which passes through all ferrites.

Half-current pulses are passed through the Z-winding and their effect on all the ferrites is opposite to that of the X and Y half-currents.

After termination of the train, which is developed in the translator section, a train end pulse is introduced into the memory which constitutes a command for the memory cycle. The first event to occur is the resetting of the adder, next the read-out, the adding of one, followed by read-in and, finally, the clearing of the ring counters in the channel programming section.

For a matrix whose operation is based on the coincidence of two half-currents, ferrites with a large degree of squareness of the magnetization curve are required. Hence, memory systems were proposed in which ferrites of poor magnetization loop squareness and wide dispersion of other parameters could be employed.

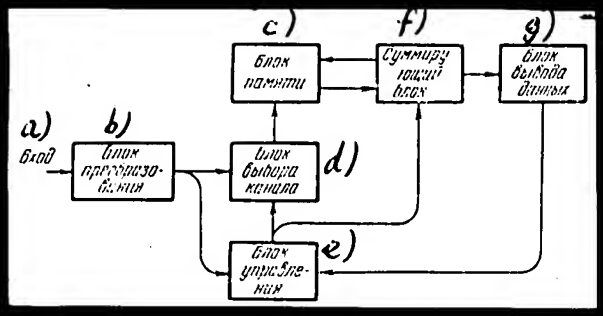

Fig. 1

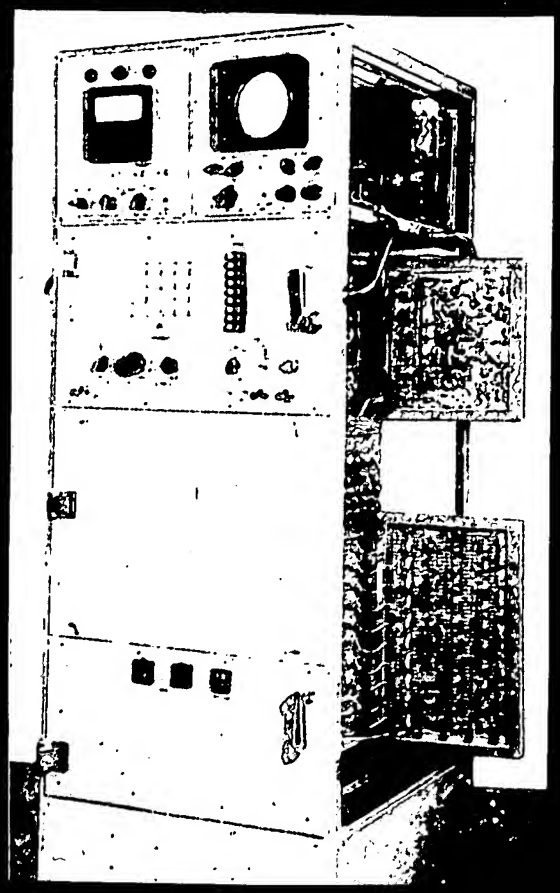

Fig. 2

Fig. 6

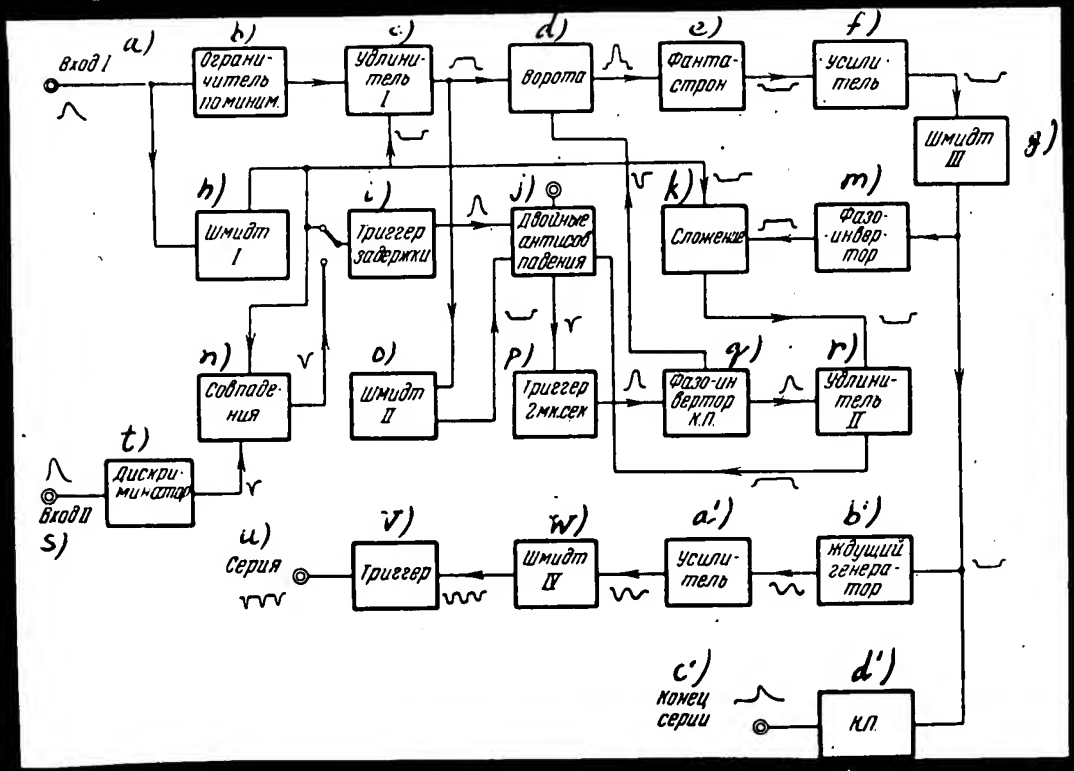

Fig. 1. Analyzer block diagram. Legend: a) Input; b) translator section; c) memory section; d) channel selector section; e) programming section; f) adder section; g) data output section.

Fig. 2. General view of the analyzer.

Fig. 6. Input signal translator block diagram. Legend: a) Input I; b) minimum level limiter; c) pulse stretcher I; d) gate; e) phantastron; f) amplifier; g) Schmidt III [Translator's Note: shaper or clipper]; h) Schmidt I; i) Delay trigger; j) double anti-coincidence; k) summing; m) phase inverter; n) coincidence; o) Schmidt II; p) 2 microsec trigger generator; q) phase inverter, cathode follower; r) pulse stretcher II; s) input II; t) discriminator; u) train; v) trigger; w) Schmidt IV; a') amplifier; b') keyed oscillator; c') pulse train end; d') cathode follower (c.f.).

Total Current System. Fig. 4 a shows a block diagram of a memory in which the ferrites constitute purely memorizing elements.

The function of selecting the specific element is performed by the system of double coincidence in the saturated cores and diode grid. Three conductors pass through each ferrite: the vertical or read-out winding, the horizontal or output winding and a read-in winding. The read-in winding is connected through its own diode for each ferrite to the corresponding horizontal and vertical write-in buses. For the read-out of the number registered in each channel square current pulses are fed into the primary winding of the saturated transformer Tk. The working principle of the saturated transformer is shown in Fig. 4C [3].

With magnetic reversal of the core Tk, a current pulse will appear in the read-out winding of the selected channel. The amplitude of the current pulse is sufficient to turn-over to 0 any ferrite in the given channel. Pulses, induced by read-out in the output windings, are passed through an amplifier to the adder section. After read-out all the ferrites in the selected channel are found to be turned-over to 0. Read-in occurs at the moment of termination of the rectangular pulses in the primary windings of Tk.

Concurrently with this, pulses of a polarity opposite to that of read-out, are induced in the secondary winding of Tk. The read-out winding is effectively disconnected due to the diode.

To write-in one in a given section a rectangular pulse is fed from transformer Tp of the adder circuit to the horizontal read-in bus. The pulse is fed into the vertical bus from the secondary winding of transformer Tk.

Fig. 4,D shows an equivalent circuit diagram of write-in pulses. The ends of the circuit are connected to low impedance sources of voltage U; under normal conditions the diode does not conduct. It is only on coincidence of the rectangular pulse from Tp with a pulse from Tk, that a write-in current pulse appears in the circuit. The amplitude of this pulse is sufficient for the writing of one. Thus read-in and read-out are performed by total current. A pulse is induced in the output windings on read-out from a single ferrite. Thus it is not distorted by superposition from partially excited ferrites as was the case in the matrix considered above.

If ferrites for such a matrix were selected by amplitude of output pulses, strobing (gating) would not be required. In this type of matrix, ferrites of poor B-H curve squareness can be used. Data will not be lost, since in a given channel ferrites are not subject to any significant excitation from one cycle of registration to the next.

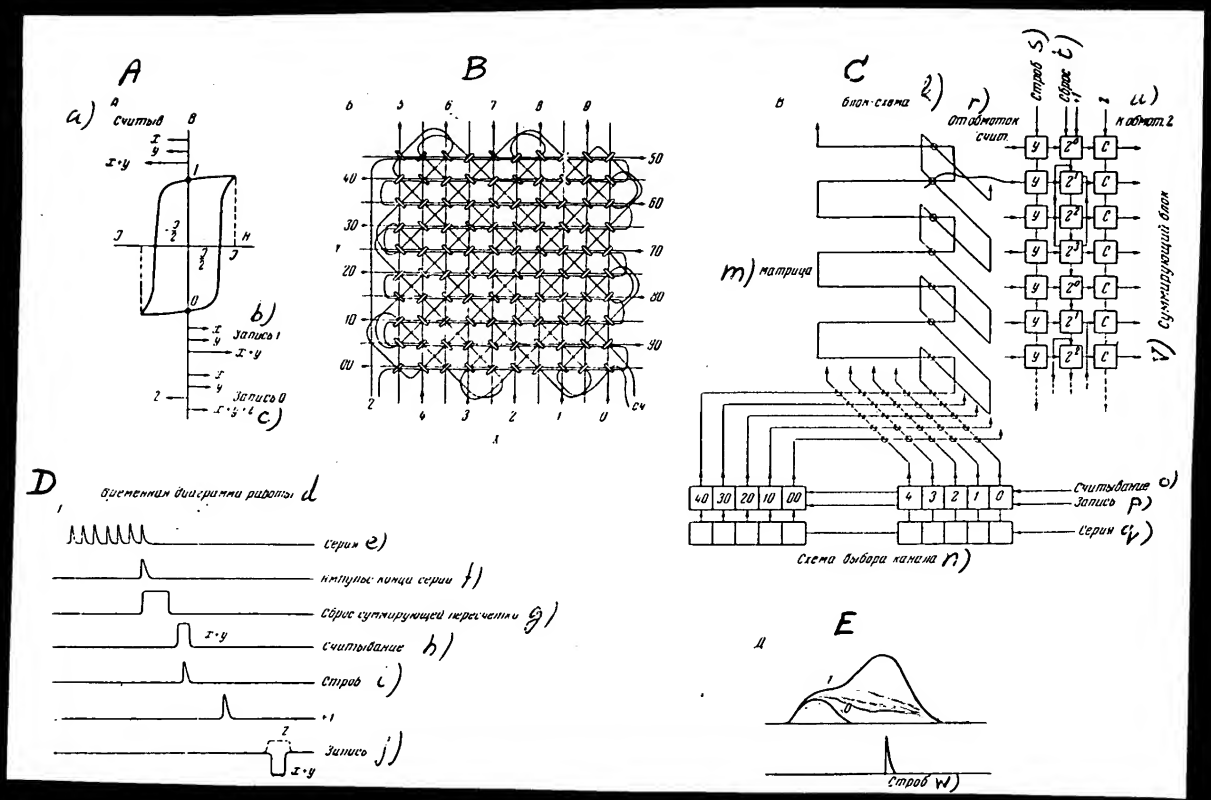

Fig. 3. Double current coincidence matrix. Legend: a) Read-out; b) read-in (write) 1; c) read-in (write) 0; d) time diagram of operation; e) pulse train; f) train end pulse; g) adder counter reset; h) read-out; i) strobe; j) read-in (write); k) block diagram; m) matrix; n) channel selector section; o) read-out; p) read-in (write); q) pulse train; r) read-out winding; s) strobe; t) reset; u) to winding Z; v) adder section.

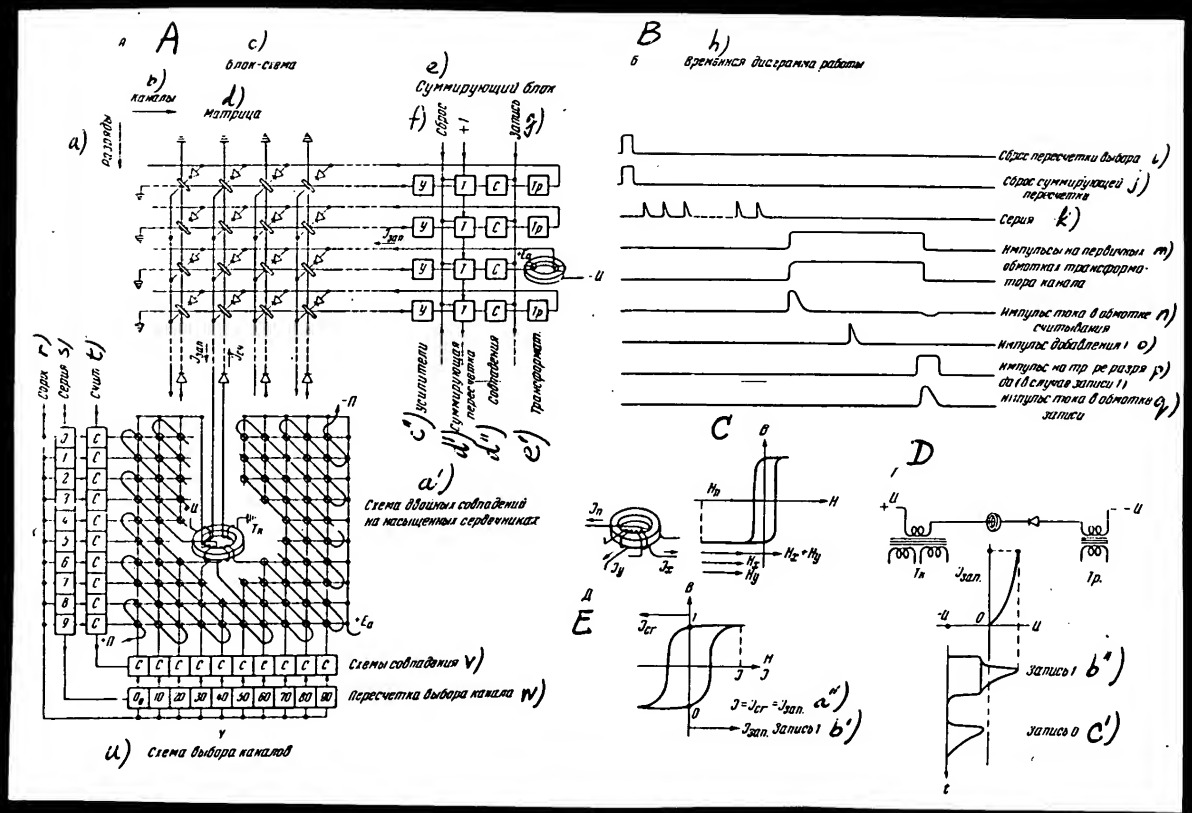

Fig. 4. Total current matrix. Legend: a) Discharges; b) channels; c) block diagram; d) matrix; e) adder section; f) reset; g) write; h) time sequence of operation; i) counter selector reset; j) adder counter reset; k) pulse train; m) channel transformer primary pulses; n) current pulse in the read-out winding; o) "addition of one" pulse; p) discharge trigger pulse (for write of 1); q) current pulse in the write winding; r) reset; s) pulse train; t) read-out; u) channel selector circuit; v) coincidence circuits; w) channel selector counter; a') saturated core double coincidence circuit; a") $I_{\text{зап}} = I_{\text{сч}} = I_{\text{сер}}$; b') Iwr. Write 1; b") write 1; c') write 0

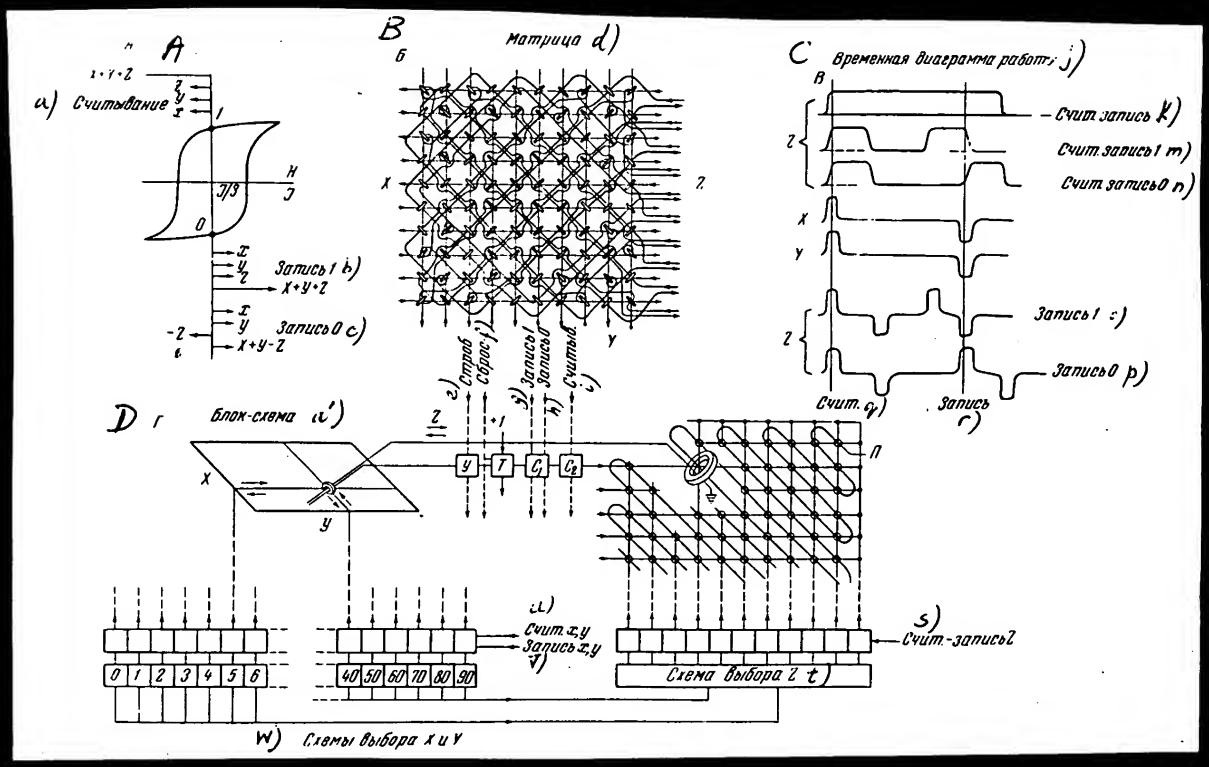

Fig. 5. Triple current coincidence matrix. Legend: a) Read; b) write 1; c) write 0; d) matrix; e) strobe; f) reset; g) write 1; h) write 0; i) read; j) time sequence of operation; k) read write; m) read write 1; n) read write 0; o) write 1; p) write 0; q) read; r) write; s) read-write Z; t) Z selection circuit; u) read x,y; v) write x,y; w) X and Y selection circuits; a') block diagram.

Triple Current Coincidence System. As shown in Fig. 5,A, ferrites of a low order of B-H curve squareness, are required for a system using triple current coincidence for core selection. Fig. 5,B shows a diagram of a thin (10 × 10) matrix. There are three groups for 10 windings X, Y and Z. For any two X and Y windings there is a Z winding which passes through only one ferrite with coordinates XY. The necessary system of Z selection is, in this configuration, controlled from the circuits selecting X and Y, and can be executed by means of diodes. For read-out from a given ferrite it is necessary to select its coordinates X, Y, Z and to pass through corresponding windings current pulses of 1/3 amplitude and of required polarity. To write-in one on the selected ferrite it is necessary to supply pulses X, Y, and Z of the same polarity, and to write-in zero, Z pulses of opposite polarity are applied. For this reason, the system of inclusion of Z is carried out with saturated cores and is controlled from the Z selector circuits and the adder section.

Fig. 5,D shows a block diagram of the memory system under consideration and Fig. 5,C shows a time sequence of its operation.

INPUT SIGNAL TRANSLATOR OF THE AMPLITUDE ANALYZER

The input signal translator performs the following basic functions.

1. Conversion of input signal amplitude into duration.

2. Blocking of the analyzer input during the translation and registration period.

3. Blocking of the analyzer input in the event of the input signal exceeding an established level (maximum limiting).

4. Blocking of the analyzer input after the input signal rises to the stipulated amplitude level, until the voltage at the input falls to zero.

5. Admittance of the input signal exceeding an established level of rejection (minimum limiting).

6. Control by the admittance circuitry of the signal under investigation originating from the external pulse.

A block diagram of the translator is shown in Fig. 6. The input signal from a pulse amplifier enters the minimum limiter circuit. In this circuit, an arrangement is provided for enhancing the linearity of the discriminator characteristic. After the limiter, the input signal is retained in the pulse stretcher circuit. Blanking of the input signal is accomplished in the admittance circuit, through which the signal does not pass in the initial condition.

From the admittance circuitry the signal is fed to an arrangement which converts the input signal amplitude into duration. From the pulse thus obtained a keyed sinusoidal oscillator is gated on. After shaping, the train of standardized pulses is fed to the channel distribution section. Non-linear pulse transformations are achieved in the second part of the diagram. From Schmidt circuit I [Translator's Note: clipper or shaper] a pulse of duration equal to that of the input pulse is applied to Pulse Stretcher I, to the delay trigger and to the summing circuit. In the summing circuit, a pulse of the same width as the input signal is added with the signal obtained after shaping in Schmidt III. The pulse thus obtained controls the admittance circuit whereby is achieved the blocking of the analyzer input for the duration of conversion and for the time required for the input voltage to fall to zero. The delay trigger is fired by the leading edge of the pulse output of Schmidt I. From the delay trigger the pulse is fed through a double anti-coincidence circuit

to another trigger generator. The resulting pulse controls the admittance circuit and Pulse Stretcher II. The restoring circuit of Pulse Stretcher II is controlled by a signal from the summing circuit. Schmidt II feeds a pulse into the double anti-coincidence circuit. The threshold of the tracking relay is determined by the desired level of maximum amplitude limiting. The blocking of the circuitry for the duration of registration is achieved by the addition of an auxiliary signal to the double anti-coincidence circuit.

ADDER, DATA OUTPUT, CHANNEL SELECTOR AND PROGRAMMING BLOCKS

The adder consists of five decades executed according to the 8 + 2 scheme. The channel selector employs two ring counters each with a cycle of 10. The first grid-coupled ring counter has a resolution time of 1 microsec, and the second cathode-coupled counter has a resolving time of 10 microsec. The data output block is engineered with circuits analogous to those described in literature [2].

TECHNICAL CHARACTERISTICS OF THE AMPLITUDE ANALYZER

The number of channels is 100. The capacity of each channel is 10^5. Channel width is 0.5 and 1 in. Dead time depends on the amplitude of the input signal and varies from 25 to 125 microsec. The data is presented on a cathode ray tube or is read out on neon indicators. The total number of tubes is 350. Power consumption is 2 Kw. The size of the analyzer is 600 × 700 × 1600 m^3. The apparatus permits distortionless examination of a spectrum when 5×10^4 randomly distributed pulses per second are applied to the input.

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LITERATURE CITED

[1] Wilkinson, D. H., Proc. Camb. Phil. Soc., 46, 508 (1950).
[2] Byington, W. Preston, and Johnstone, C. Wilkin, "100-Channel Amplitude Analyzer with Magnetic Core Memory," (Material presented by the Los Alamos Laboratory at the International Conference on the Peaceful Uses of Atomic Energy, 1955).
[3] Rajchman, J. A., Proc. IRE, 41, 1407 (1953).